WHAT IS CLAIMED IS:

1. An electronic camera in which an analog signal output from an image pickup device is AD-converted and digital processing is performed on the AD-converted signal on the basis of a basic operating clock, said camera comprising:

clock change device of changing the frequency of the basic operating clock; and

control device of controlling the clock change device so that the frequency of the basic operating clock is reduced at the time of AD conversion of a still image output from the image pickup device.

2. The electronic camera according to claim 1, further comprising photometry device of measuring the brightness of a subject, wherein said control device controls the clock change device so that the frequency of the basic operating clock is reduced when it is determined that the brightness of the subject measured by said photometry device is lower than a predetermined brightness.

3. The electronic camera according to claim 1, further comprising photography mode selecting device of selecting a desired photography mode from a plurality of photography modes, wherein said control device controls the clock change device so that the frequency of the basic operating clock is reduced only when a particular one of the photography modes is selected by said photography mode selecting device.

4. The electronic camera according to claim 1, further comprising ISO speed setting device of setting an ISO speed, wherein said control device controls the clock change device so that the frequency of the basic operating clock is reduced when the ISO speed set by said ISO speed setting device is equal to or higher than a predetermined value.

5. The electronic camera according to claim 1, further comprising first and second line memories in which the AD-converted digital signal is alternately stored in a predetermined data amount, and a RAM for temporarily storing the digital signal at least for one frame of a still image, wherein, when capture of the digital signal in said first line memory is completed, the captured digital signal is DMA-transferred to said RAM on the

basis of the basic operating clock, and wherein, when capture of the digital signal in said second line memory is completed, the captured digital signal is DMA-transferred to said RAM on the basis of the basic operating clock signal.